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Commissioner for Patents
P. O. Box 1450
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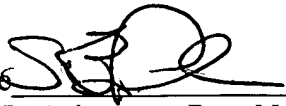
SUBJECT: Serial #: 10/767,275
File Date: 01/29/04
Inventors: Ming Fu Li
Examiner: Nadav, Ori.
Art Unit: 2811
Title: CMOS Compatible Low Band Offset Double
Barrier Resonant Tunneling Diode

RESPONSE TO OFFICE ACTION

In response to the Office Action of 06/14/05 please amend the above identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents
P. O. Box 1450, Alexandria, VA 22313-1450 *October 14, 2005*

Signature 
Stephen B. Ackerman, Reg. No. 37,761

Date: 10/14/05

Amendments to the Claims are reflected in the listing of claims that begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.